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PERFORMANCE IMPROVISATION INSIDE CACHE TILE USING MAPPING ALGORITHM

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Abstract

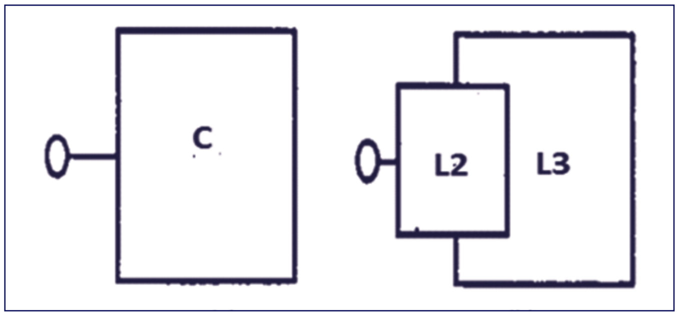
There is huge demand for improvisation of cache memory performance considering multiprocessors. Cache memory arranged in tile fashion. These cache tiles are placed in multiple levels. Here work involves survey of existing search algorithm to draw conclusions and to develop algorithm which reduces number of searches required. There by improvisation performance parameter latency. Latency reduction is achieved by avoiding unnecessary search through all location.

Keywords: Cache memory, Search algorithm, latency.

INTRODUCTION

Many applications including mobile and processors demand cache with high performance. Uniform cache architecture performance fig 1(a) is poor due to wire delay problem. Multiple level cache fig 1(b) helps to improvise performance by providing parallel access.

Figaure 1(a) UCA Figaure 1(b)ML-UCA

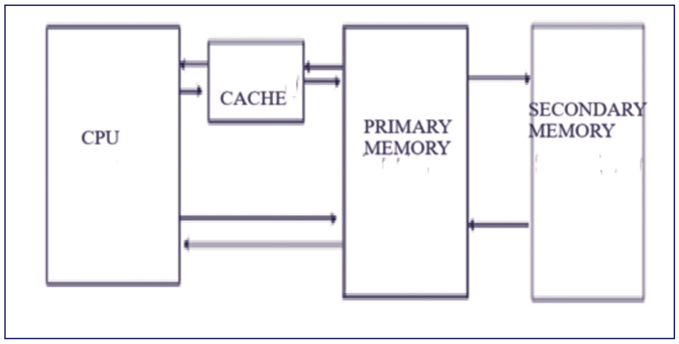


Cache is small and temporary memory that exist in between processor and main memory as shown in figure 2.

Multiple Levels of Memory:

1) Register – Registers exist on chip. These are fastest memory. Common registers available are accumulator, PC-program counter, Stack pointer/address register etc.
2) Cache memory – This is the memory we are working on. Here in cache data is stored temporarily with the advantage smaller access time. Hence it is the fastest memory.
3) Main Memory – It is a volatile memory; Size is large compared to cache. Less fast compared to cache.
4) Secondary Memory – It is non-volatile in nature. Speed is less compared to RAM but it has the advantage of storing data permanently. Key points to be considered during search inside cache are: 1) Hit: The address to be searched present in cache. 2) Miss: The address to be searched not found in cache.

Figure 2: CPU with multiple levels of memory



Cache Mapping: Data mapping is categorised into three types in cache memory. Direct, Set-Associative and Associative mapping. Here the design is made using direct mapping technique. Direct-Mapping is simplest way of mapping. It maps each main memory block into only specified cache memory line. The previous block is trashed when another main memory block needs to be loaded to same place. Address of cache is divided into tag and index field. Tag is stored in cache. The remaining part of address is same as main memory address.

i = n modulo m

i=cache memory line number

n= RAM block number

m=Total number of cache lines

BACK GROUND WORK

Acharya [1] presents cache trie search algorithms. There are main three important features that exist for this algorithm. B tree hash table vector using data structure is developed for each node. considering cache characteristics and the fan-out of the node, data structure is decided. Changing the data structure design in dynamic fashion, they adapt to changes in the fanout. The layout and size of data structure is depends on size of symbols in alphabet. Brodal [2] presents a cache-oblivious algorithm. In this algorithm there is no multiple cache hierarchy. Design is considered with only one level of memory. The design does not consider or it does not have knowledge of memory hierarchies. Design is analyzed in a two-level I/o model. Hence result or algorithm can be applied to multi-level hierarchies. search tress has search cost O is log $_B$N I/O s and it has search cost same as B-trees. Real-time indices are the aspects of modern search engines. These get incorporated the change in content within seconds. These search engines help to reduce user latency and back-end load. CIP – the cache invalidation predictor [3] is an architectural component. Researcher discuss cache memory replacement techniques. LRU-Least recently used technique fails to work with freshness over time and CIP gives better results with 97 percent of queries with fresh results. T. C. Xu [4] work on mapping algorithm considering big data applications. Data processing is on demand. Data needs to be processed very fast. Work is to explore characteristics of data applications with multi core processor and shared cache. Performance metrics considered is latency. Belady's algorithm [5] is an optimal solution. This algorithm is infeasible as it needs understanding of the future. The researcher justifies that the algorithm is efficient way, as it introduces a unique way for efficiently simulate Belady's behavior and to represent the long history information they have used a known sampling technique that is needed achieve high accuracy.

This paper [6] explain a algorithm is to implement, deployment experience of cache stack. Cache traffic is portioned into disjoint categories by cache stack and analyze the benefit for cache from each subset. Knapsack problem is formulated to match the best admission policy to each cache set. Tree-based backtracking search [7] is a technique to find solution for distributed constraint optimization problem. Here there is effective reuse of historical search. Hence, reducing the overall overhead. This paper proposes Retention Scheme (RS) for tree-based synchronous backtracking search. Javier marino [8] presents dynamic cache partitioning. Divides L2 bank into a private and shared partition. Placing private data closure to core processor. Depending on the work load proposed architecture self adjust the sharing partition.

Cache indexing policy [9] reduces the conflict misses. Indexing policy spreads the references to the all-cache memory sets. Power consumption is the performance parameter considered. Merino, V [10] proposed Enhanced Shared-Private Non-Uniform Cache Architecture (ESP-NUCA), which is suitable for high performance processor and it is also cost effective. During run time to determine the cache memory configuration the approaches are introduced. These approaches are based on algorithms to test cache configuration in variety of orders [11, 12, 13,14, 15]. Energy consumption estimations with mathematical model are used to determine cache performance during runtime [11,12,13,15] or to find cache miss rate[14]. Reconfiguration is made according to selected configuration candidate. Then comparison is made between previous one and reconfigured cache. Conclusion is drawn.

DESIGN

Considering physical address bits as 12 bits. One cache tile has 32 locations. There exist eight blocks. Each block contains four bytes.

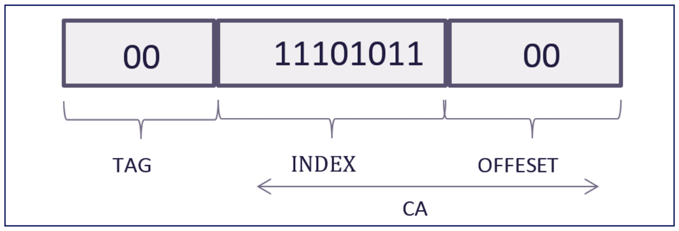
Offset bits are $\log_2$ (number of words per block) = $\log_2(4)$=2

Index bits are $\log_2$ (number of blocks in cache) = $\log_2(256)$ =8

Tag bits=Physical address-offset bits-Index bits=2

As each tile has 32 location, always upper 5 bits of Index remain same. Hence, it reduces 32 location address comparison to 1 comparison. Hence this search algorithm by using direct mapping improves performance.

Figure 3: Physical address



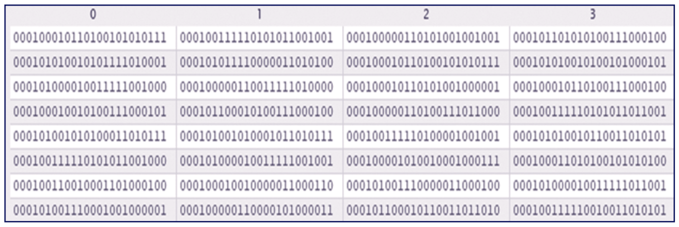
TAG: TAG bits

CA=INDEX bits + offset bits

DATA=Data bits of cache

RESULTS

Figure 4: Stored memory of a tile

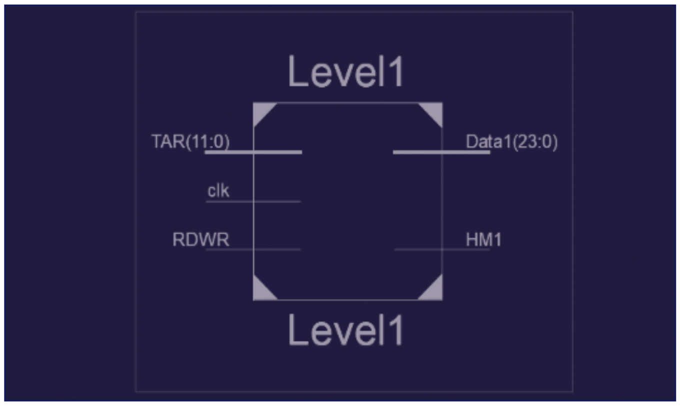


0	1	2	3
000100010110100101010111	000100111110101011001001	000100000110101001001001	000101101010100111000100
000101010010101111010001	000101011110000011010100	000100010110100101010111	000101010010100101000101
000101000010011111001000	000100000110011111010000	000100010110101001000001	000100010110100111000100
000100010010100111000101	000101100010100111000100	000100000110100111011000	000100111110101011011001
000101001010100011010111	000101001010001011010111	000100111110100001001001	000101010010110011010101
000100111110101011001000	000101000010011111001001	000100001010010001000111	000100011010100101010100
000100110010001101000100	000100010010000011000110	000101001110000011000100	000101000010011111011001
000101001110001001000001	000100000110000101000011	000101100010110011011010	000100111110010011010101

Figure 4 shows memory picture of the cache tile with twenty four bit data stored. There are eight blocks with each block containing four locations. Figure 6 Search algorithm experiencing hit in tile1 with HM_Le1 going high. Hence data reflected on DATA bits otherwise it will be unknown.

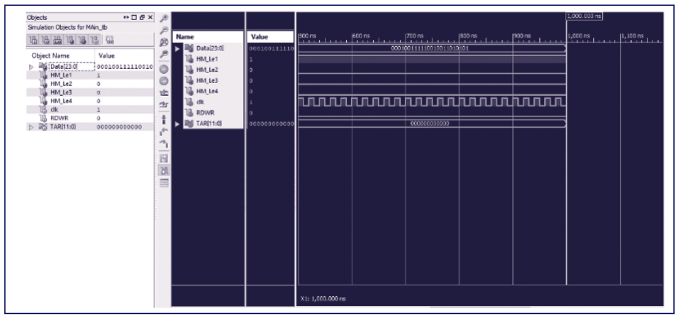
RTL schematic of tile is shown in figure 5. Address to be searched is sent through TAR _Test Address Register. RDWR represents weather operation related to read or writing data from or to cache memory. Data1 will have 24-bit data if search experience hit otherwise, it remains empty. HM1 represents weather tile experience hit/miss.

Figure 5: RTL Schematic of a tile



TAR: Test Address Register
clk: Clock
RDWR: Read/Write operation
HM1: Hit or Miss in Tile
Data: Data if tile has experienced hit
Tool used: Xilinx ISE

Figure 6: Simulation results



Object Name	Value
Data[23:0]	000100111110010
HM_Le1	1
HM_Le2	0
HM_Le3	0
HM_Le4	0
clk	1
RDWR	0
TAR[11:0]	000000000000

HM_Le1:1=hit,0=miss

Data: Data from location where hit occurred

TAR: Search address

Figure 6 depicts search through tile_1 experiencing hit . Hence HM_Le1 is high and data from location where hit has occurred is reflected on to data lines.

CONCLUSION

The design of cache tiles helps to avoid unnecessary search. The design uses direct mapping technique. The design of tile is such that it removes thirty one comparisons of index bits and helps to improve the performance by reducing latency. Performance improvisation by reducing latency is the very important when it comes application of cache memory which is achieved with minimum Gate delay of 0.575 ns.

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